Super Junction MOSFET series

Benefits given by R60xxJNx series for the Phase-Shift Full-Bridge

The full-bridge configuration is utilized for power supplies such as server power sources, on-board chargers, and many other power electronic applications. In particular, the phase-shift full-bridge circuit (PSFB) enlarges its power supply capability through reduced switching losses, because this circuit topology allows the adoption of zero-voltage switching (ZVS) techniques for switching devices such as SJMOS and IGBTs. This application note explains how the PSFB equipped with SJMOS’s operates, and also elucidates why SJMOS in the PSFB must have high-speed recovery capability for its body diode (BD). In addition, this document provides the measurement results of power conversion efficiency for the PSFB including ROHM’s PrestoMOS™ and competitor’s SJMOS, and finally proves that our R60xxJNx series realizes the best power conversion efficiency of the PSFB.

Basic Circuit Configuration of PSFB

Figure 1 shows the fundamental schematic of the PSFB. The leakage inductance of the transformer working as the resonant inductor enables ZVS, while an additional inductor is often serially connected to the transformer in order to expand the ZVS operating area. The PSFB in this application note always includes this kind of additional inductor, $L_s$.

Figure 2 shows the ON/OFF timing chart of switch Q1 to Q4. The numbers at the bottom of the figure label represent the specific operation modes of the circuit. As shown in this diagram, the ON/OFF timing of Q3 and Q4 always comes after the ON/OFF timing of Q1 and Q2 with a specific phase delay. Thus, in general, the leg of Q1 and Q2 is named the leading leg, while the leg of Q3 and Q4 is named the lagging leg.
Basic Operation of PSFB

ZVS in PSFB is achieved by turning on a MOSFET with a forward current flowing through its body diode (BD) so that its output capacitance of the MOSFET ($C_{oss}$) is fully discharged.

Figure 3 includes the waveforms of drain current ($I_D$) of Q1 to Q4 as well as the current flowing through the primary-side transformer ($I_L$) under normal operating conditions. The direction of drain-to-source is defined as the positive direction of $I_D$ here, and you can easily find the period that minus $I_D$ flows in each Q1 to Q4 with its BD being forward biased. During this period, the drain voltage is nearly zero, leading to ZVS if the MOSFET is turned on.

![Figure 3. $I_D$ for Q1 to Q4 ($I_{D_{Q1}}$, $I_{D_{Q2}}$, $I_{D_{Q3}}$, $I_{D_{Q4}}$), and $I_L$.](image)

As you can see in Figure 3, the current waveforms are not the same for the leading and lagging leg in spite of the same operating pattern. You can get the picture of why the waveforms differ by grasping how current flows in mode (1)-(14) defined in Figure 2 and 3. The following Figure 4 to 7 explain current path step-by-step for each mode, for a better understanding of the waveforms in Figure 3.

**Mode 1**
- Q1 and Q4 are on-state, whereas Q2 and Q3 are off-state.
- The off-state of Q2 and Q3 means that the output capacitance of Q2 ($C_{oss_{Q2}}$) and of Q3 ($C_{oss_{Q3}}$) are fully charged.
- $V_i$ is applied to the primary side of the transformer.
- The energy is stored in $L_s$ by the current flowing through it.

**Mode 2**
- Q1 turns off.
- The output capacitance of Q1 ($C_{oss_{Q1}}$) is being charged. Due to this, the drain-side voltage of Q2 drops, which triggers discharging of $C_{oss_{Q2}}$.
Mode (3)

- If \( L_s \) still holds the energy after charging \( C_{oss,Q1} \) and discharging \( C_{oss,Q2} \) are completed, the BD of Q2 (D\(_{Q2}\)) is forward biased, starting its freewheeling phase.
- In the freewheeling period, the energy isn’t delivered to the secondary side. However, the current on secondary side continues to flow due to \( L_s \). So, the forward current flows through D1 and D2.

Mode (4)

- Q2 turns on. At this point, D\(_{Q2}\) is on-state, and this means that the drain-source voltage of Q2 (\( V_{DS,Q2} \)) is almost zero. Thus ZVS is achieved, leading to little turn-on loss.

Mode (5)

- Q4 turns off.
- The output capacitance of Q4 (\( C_{oss,Q4} \)) is being charged. Due to this, the source-side voltage of Q3 drops, which triggers discharging of \( C_{oss,Q3} \).

Mode (6)

- If \( L_s \) still holds the energy after charging \( C_{oss,Q4} \) and discharging \( C_{oss,Q3} \) are completed, the BD of Q3 (D\(_{Q3}\)) is forward biased, starting freewheeling.

Mode (7)

- Q3 turns on. At this point, D\(_{Q3}\) is on-state, and this means that the drain-source voltage of Q3 (\( V_{DS,Q3} \)) is almost zero. Thus ZVS is achieved, leading to little turn-on loss.
- This voltage direction makes current flow opposite to \( I_L \) in Mode (1) to (6), and consequently the current direction flips rapidly.

Figure 5. The Current path in Mode (3) - (7)
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Mode (8)

- Q2 and Q3 are on-state, whereas Q1 and Q4 are off-state.
- The off-state of Q1 and Q4 means that $C_{oss\_Q1}$ and $C_{oss\_Q4}$ are fully charged.
- $V_i$ is applied to the primary side of the transformer in the opposite direction.
- The energy is stored in $L_s$ by current flowing through it.

Mode (9)

- Q2 turns off.
- $C_{oss\_Q2}$ is being charged. This triggers discharging of $C_{oss\_Q1}$.

Mode (10)

- If $L_s$ still holds the energy after charging $C_{oss\_Q2}$ and discharging $C_{oss\_Q1}$ are completed, the BD of Q1 ($D_{Q1}$) is forward biased, starting freewheeling.
- In the freewheeling period, the energy isn't delivered to secondary-side. However, the current continues to flow due to $L_o$. So, the forward current flows to D1 and D2.

Mode (11)

- Q1 turns on. At this point, $D_{Q1}$ is on-state, and this means that the drain-source voltage of Q1 ($V_{DS\_Q1}$) is almost zero. Thus ZVS is achieved, leading to little turn-on loss.

Mode (12)

- Q3 turns off.
- $C_{oss\_Q3}$ is charged, while $C_{oss\_Q4}$ is discharged.

Figure 6. The Current path in Mode (8) - (12)
As detailed in explanation for Mode (7) and (14), the turn-on of a MOSFET in the lagging leg causes the serial connection of the input source and \( L_s \), and thus the energy stored in \( L_s \) diminishes rapidly. This operation mode does not happen for the leading leg, and consequently the waveforms differ between the leading and lagging leg. As explained for Mode (5), (6), (12), and (13), in the lagging leg, if the energy stored in \( L_s \) is less than the one stored in \( C_{\text{oss}} \), a MOSFET cannot complete the charging and discharging process and ZVS cannot be achieved. Hence, if Mode (5) is taken as an example, the condition to establish ZVS is expressed as equation (1).

\[
\frac{1}{2}L_s i_{L1}^2 > E_{\text{oss},Q3} + E_{\text{oss},Q4}
\]  

(1)

Where \( i_{L1} \) is \( i_L \) at the point that Mode (4) completed, and \( E_{\text{oss},Q3} \), \( E_{\text{oss},Q4} \) is the energy necessary to charge the \( C_{\text{oss}} \) of Q3 and Q4, respectively.

Equation (1) shows that ZVS is not achieved for small \( i_L \), namely light load, and also that it become easier to establish ZVS for heavier load.

**Remarks for device operation in the case of light load**

As explained in details above, small current in light-load operation causes low energy storage in \( L_s \), and consequently a MOSFET in the lagging leg highly likely switches without completing its charging and discharging process. This results in no ZVS operation and consequently increases the turn-on loss of the MOSFET.

On the other hand, MOSFETs in the leading leg transfer energy to the secondary side through the transformer during their charging and discharging transitions. Similar consideration for deriving equation (1), if we take Mode (2) as an example, leads to the condition to achieve ZVS in the leading leg as:

\[
\frac{1}{2}(L_s + n^2L_o)L_2^2 > E_{\text{oss},Q1} + E_{\text{oss},Q2}
\]  

(2)

Where \( n \) is the turns ratio of the transformer, \( L_2 \) denote \( L \) at the final stage of Mode (1), \( E_{\text{oss},Q1} \) and \( E_{\text{oss},Q2} \) defines the energy necessary to charge or discharge \( C_{\text{oss}} \) of Q2, respectively.

Setting of the dead time is needed to avoid short circuit of high-side and low-side arms for practical circuit operation. On the other hand, \( V_{\text{oss}} \), as mentioned above, possibly remains non-zero under a light load condition due to incompletion of discharging the...
MOSFETs in the lagging leg. This means on the other side that some dead-time settings could increase the possibility of not achieving ZVS at light load operation. Therefore the duration of dead time should be adjusted carefully.

Figure 8 qualitatively illustrates the turn-on transient waveforms of \(V_{DS}\) and \(I_D\) for an optimized and non-optimized dead-time setting case.

![Figure 8. Simplified turn-on transient waveforms of \(V_{DS}\) and \(I_D\) of a MOSFET in the lagging leg.](image)

Figure 8 also shows that for a non-optimized dead-time case, a large \(I_D\) instantaneously flows. This current has two components: a short-circuit current caused by the gate-source voltage \(V_{GS}\) exceeding its threshold [1], and the current to charge the \(C_{oss}\) of the MOSFET in the other arm. This latter part is unavoidable for hard-switching operation, but you can prevent the former one by tuning appropriately the ratio of \(C_{gd}\) to \(C_{gs}\), where \(C_{gd}\) and \(C_{gs}\) denote the gate-drain and gate-source capacitance of the MOSFET respectively.

PrestoMOS\textsuperscript{TM} can suppress the short-circuit current by tuning the ratio of \(C_{gd}/C_{gs}\), and thus low power loss, namely high efficiency can be achieved.

**Remarks for device operation in the case of heavy load**

MOSFETs likely fail by unintentional triggering of the parasitic bipolar transistor embedded in a MOSFET in the leading leg, if \(t_r\) of the BD is large in the case of heavy load [1]. This spontaneous turn-on is caused by the current charging the drain-source capacitance \(C_{ds}\) when MOSFETs turn off, and thus this bipolar-oriented instantaneous large current triggers the fatal accident.

In an inverter circuit, the charge stored in a BD \(Q_{rr}\) is forcefully and quickly evacuated by the high-voltage reverse bias applied during the turn-off of the BD. The time necessary to evacuate these charges is \(t_{rr}\), which kept small in this case. On the other hand, as shown in Figure 9, the voltage applied to a BD is nearly zero during its recovery in PSFB, and therefore the stored charge needs longer to be evacuated, leading to a larger \(t_{rr}\). Figure 10 provides experimental waveforms for this phenomenon. It includes the reverse recovery current waveforms of conventional SJMOS for different drain-source voltages.

A decreasing \(V_{DS}\) and, hence a larger \(t_{rr}\) shifts the reverse recovery current as shown by the red dotted lines in Figure 9. As a result, large \(t_{rr}\) means a large amount of charges in the MOSFET during its turning off, and in this case current easily flow through the MOSFET, increasing the possibility to turn on the parasitic bipolar transistor.
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![Diagram of MOSFET operation](image)

Figure 9. Schematically drawn waveforms of $V_{DS}$ and $I_D$ of MOSFETs in the leading leg.

![Diagram of BD recovery](image)

Figure 10. Recovery characteristic of a BD as a function of $V_{DS}$.

<table>
<thead>
<tr>
<th>Drain - Source Voltage $V_{DS}$ (V)</th>
<th>Reverse recovery time $t_r$ (ns)</th>
</tr>
</thead>
<tbody>
<tr>
<td>4</td>
<td>940</td>
</tr>
<tr>
<td>16</td>
<td>510</td>
</tr>
<tr>
<td>20</td>
<td>450</td>
</tr>
<tr>
<td>400</td>
<td>420</td>
</tr>
</tbody>
</table>

![Diagram of MOSFET operation](image)

Figure 11. Schematically drawn waveforms of $V_{DS}$ and $I_D$ of MOSFETs in the lagging leg.

t0-t1: BD is forward biased after $C_{oss}$ is discharged.

t1-t3: BD turns on.

t1-t5: MOSFET turns on.

t3-t4: Recovery current of BD flows. Large $t_r$ extends this period.

t5-t6: MOSFET turns off. Large $t_r$ increase the possibility to break MOSFET by unintentional turn-on of its parasitic bipolar transistor.

t0-t1: BD is forward biased after $C_{oss}$ is discharged.

t0-t2: BD turns on.

t1-t4: MOSFET turns on.

t2-t3: Recovery current of BD flows. Large $t_r$ extends this period.

t4-t5: MOSFET turns off. The recovery operation of BD less influence the process than the BD does in the leading leg, and unintentional turn-on rarely happens.

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Power conversion efficiency

PrestoMOS™ due to their small $t_r$ is useful solutions for PSFB. However, not only a fast diode is needed, but also a high power conversion efficiency is sought. Figure 12 shows the efficiency of a PSFB power supply. MOSFETs used for Q1 to Q4 are PrestoMOS™ and competitor’s SJMOS, all of which have around 0.2Ω of on-resistance. The measurement conditions are input voltage $V_i=390V$, output voltage $V_{out}=12V$, output current $I_{out}=10A~50A$, and switching frequency $f_{sw}=100kHz$.

![Figure 12. Power conversion efficiency as a function of $I_{out}$.](image)

As shown above, R6020JNX, the newest generation of PrestoMOS™, provide best power conversion efficiency over all load conditions used for the measurement. R60xxJNx series tops in switching capability among high-speed recovery SJMOS, and also has higher gate threshold voltage $V_{GS(th)}$ than R60xxFNx series and other providers do. Generally, a high $V_{GS(th)}$ increase turn-on loss. In PSFB, however, dead-time tuning for light load and ZVS for heavy load suppress turn-on loss, minimizing the disadvantage of high $V_{GS(th)}$.

If you would like to design a PSFB with SJMOS, our R60xxJNx series fits very well the converter requirements.

Summary

- The MOSFET in the lagging leg do not take ZVS option in light load operation, and consequently turn-on loss emerges. Engineers have to adjust appropriately this turn-on loss to reduce the turn-on loss.
- In heavy load operation, large $t_r$ of MOSFET’s BD increase the risk of unintentional triggering of the parasitic bipolar transistors in the MOSFET. Therefore you have to adopt MOSFETs equipped with a small $t_r$ BD.
- R60xxJNx series are the newest generation of PrestoMOS™ with top characteristics in high-speed recovery SJMOS. High $V_{GS(th)}$ effectively reduce the possibility to cause short-circuit current, suppress turn-off loss. These features are very useful for the PSFB in which ZVS is utilized during turn-on.
References

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