

Linear Regulators

Simple Test Method for Estimating the Stability of Linear Regulators

BAxxCC0 series

No.AEK59-D1-0086-0

Low drop-out (LDO) regulators developed back in the age when large-capacitance multi-layer ceramic capacitors (hereinafter, MLCCs) were uncommon cause a phase delay, leading to oscillation when connected to a low-ESR capacitor like an MLCC. Often, MLCCs are used to save board space and prolong the lives of electronic components. A resistor placed in series in the circuit increases apparent ESR and establishes a phase lead that enable the use of an MLCC as an output capacitor. Phase margin measurement is practical on an LDO having variable output voltage, since its feedback loop is outwardly exposed. However, on a fixed output voltage LDO, the phase margin cannot be measured because of its closed loop circuit. This Application Note provides tips for estimating stability through a simple test that uses the step response method.

Common Method for Measuring Phase Margin

For LDO phase margin measurement, a signal source is placed in a part of the LDO's closed loop that is cut from the loop, then, the phase margin is evaluated on its board wiring diagram as shown in Fig. 1. This method is, however, inapplicable to an LDO of variable output voltage because of its feedback loop built in the IC.

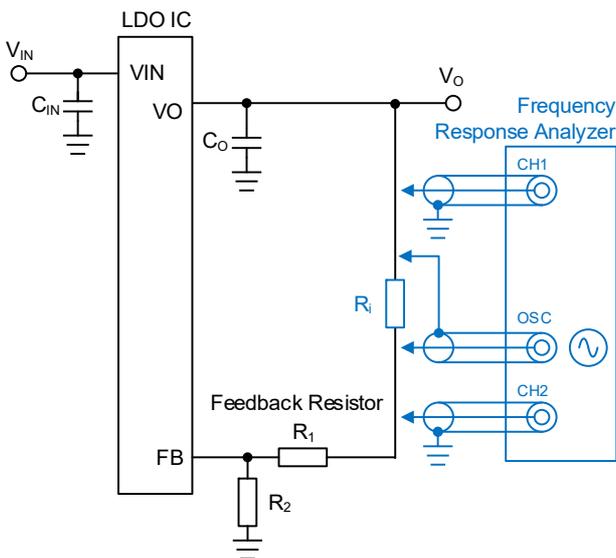


Fig. 1 Typical Circuit to Measure Phase Margin

Stability Estimate by Simple Experiment

If a board wiring diagram is unavailable, the step response method provides a simple solution for measuring the stability of the circuit. Given in Fig. 2 is an example of a circuit for measuring step response, in which an electronic load device is connected to the LDO output V_O , whose waveform is to be monitored via an oscilloscope. Power is supplied to V_{IN} of the LDO, then the current of the electronic load device is changed. For example, applying a rapid change at a slew rate of $1\text{ A}/\mu\text{s}$ to the current within the range from 0 A to the rated current of the LDO returns a typical waveform of the step response.

If no electronic load device is available, a circuit alternatively incorporating a transistor switch, as shown in Fig. 3, works effectively to measure step responses. In this circuit, a function generator is connected to the gate of an N-ch MOSFET, to quickly turn the transistor on and off. When the transistor is off, the current is at 0 A, and when it is on, a current of V_O/R_L flows.

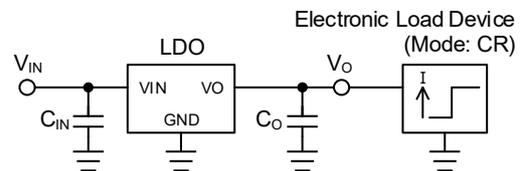


Fig. 2 Example of Circuit to Measure Step Responses

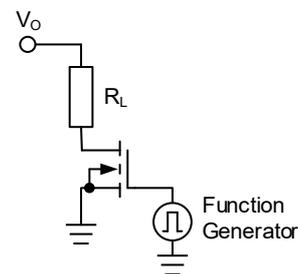


Fig. 3 Load Device Using a Transistor Switch

Using an MLCC for the output of the BA05CC0 and a resistor placed in series, a test was conducted to establish a relationship between step response and phase margin. Figure 4 shows the circuit used for step response measurement, while Figs. 5-10 provide the test results. Figures 11-17 are the results of tests in which different output capacitances were applied to the capacitor.

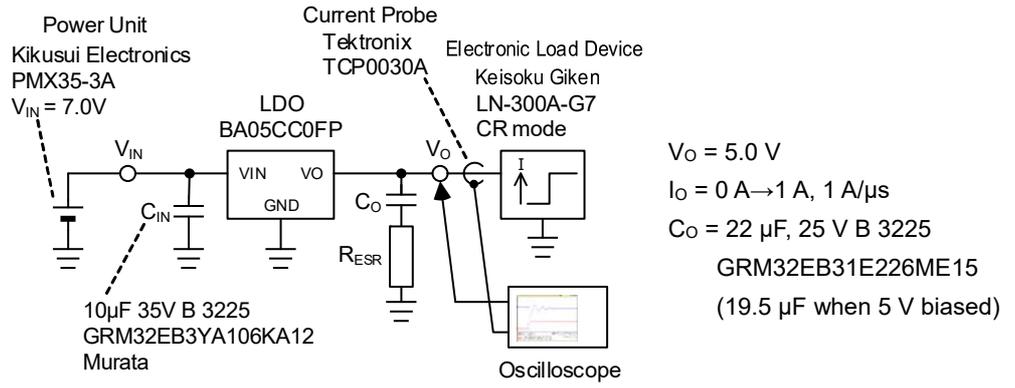


Fig. 4 Example of Circuit Used for Step Response Measurement

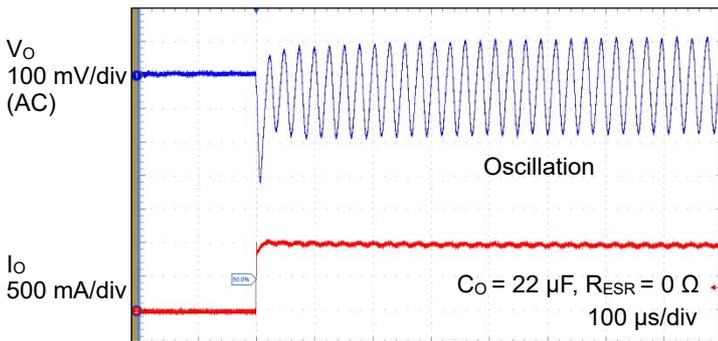


Fig. 5 Phase Margin = 0

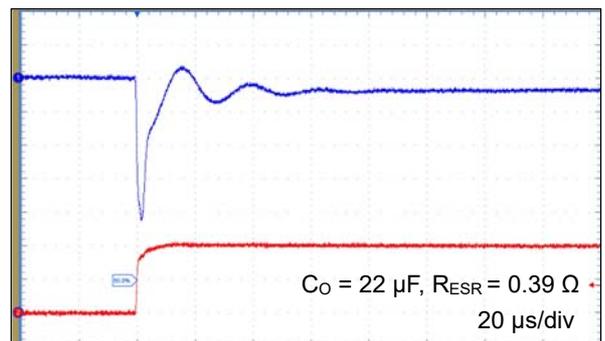


Fig. 8 Phase Margin = 52 deg

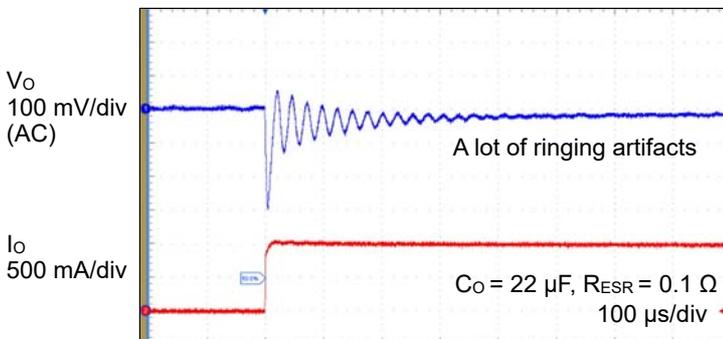


Fig. 6 Phase Margin = 9.9 deg

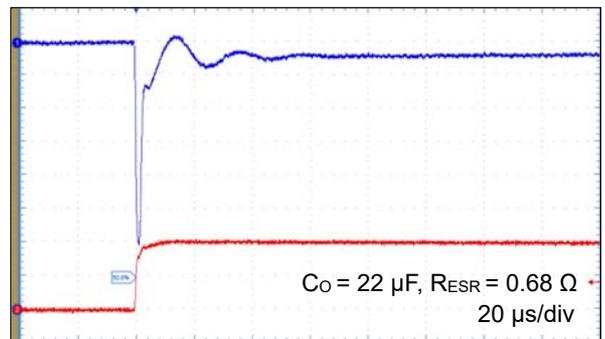


Fig. 9 Phase Margin = 82 deg

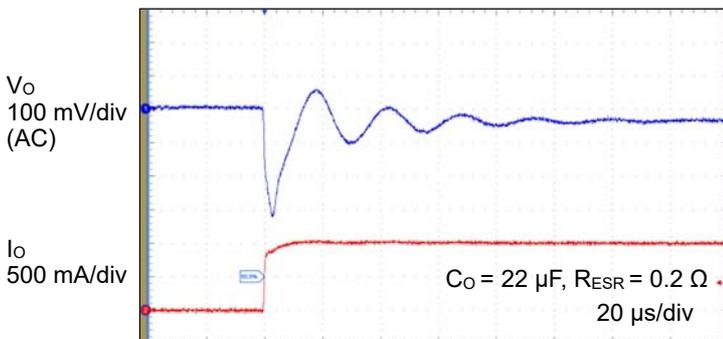


Fig. 7 Phase Margin = 25 deg

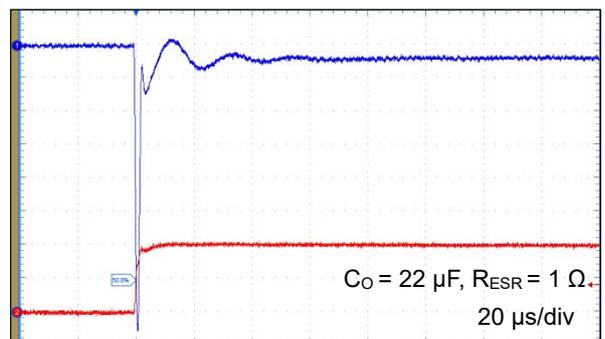


Fig. 10 Phase Margin = 70 deg

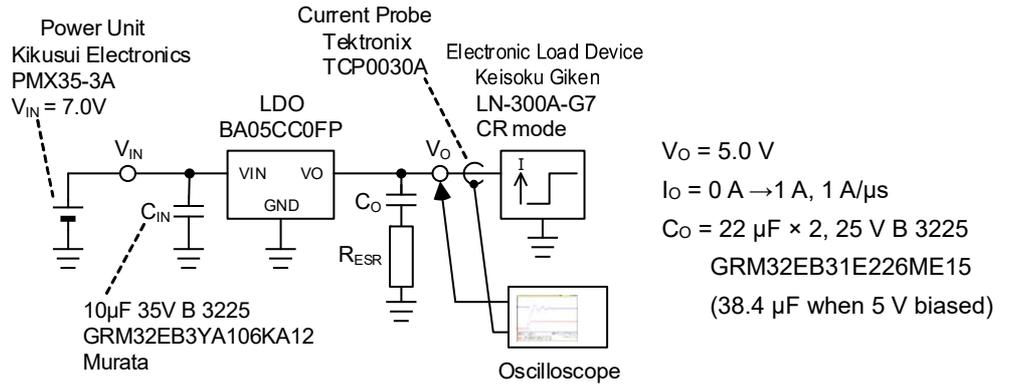


Fig. 11 Example of Circuit Used for Step Response Measurement

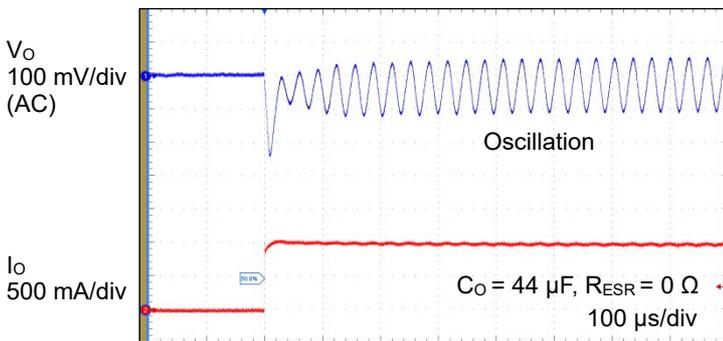


Fig. 12 Phase Margin = 0

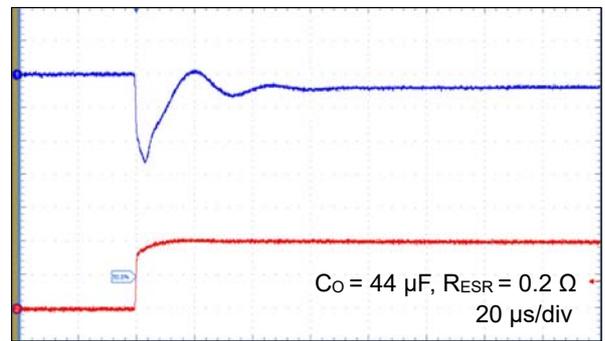


Fig. 15 Phase Margin = 38 deg

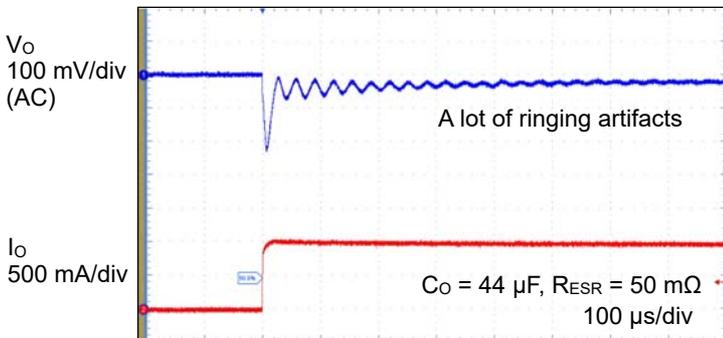


Fig. 13. Phase Margin = 10 deg

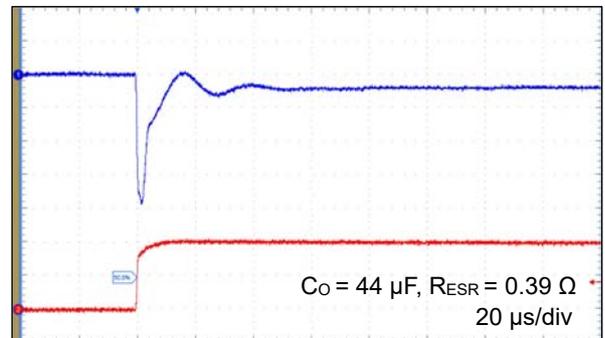


Fig. 16 Phase Margin = 60 deg

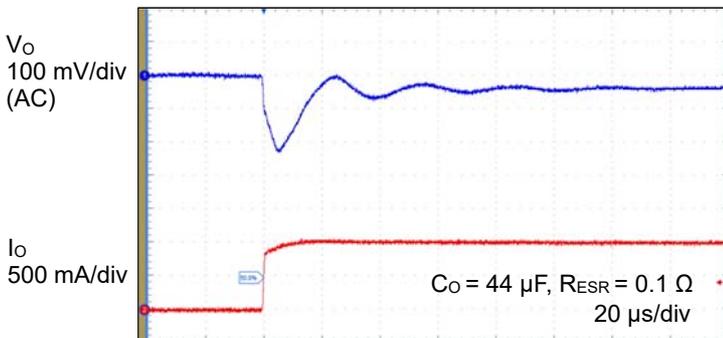


Fig. 14 Phase Margin = 19 deg

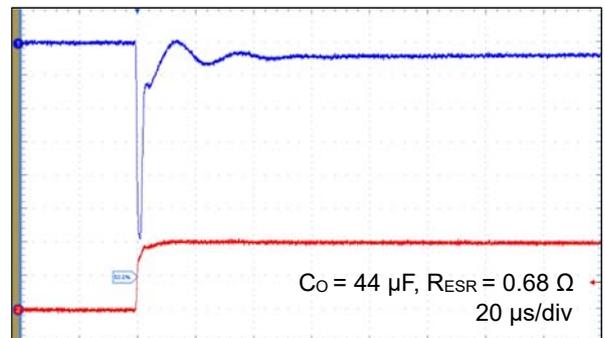


Fig. 17 Phase Margin = 85 deg

At $C_O = 22 \mu\text{F}$

Phase Margin	Ringling Cycle
9.9 deg	≥ 10
25 deg	6
52 deg	4
70 deg	3
82 deg	3

At $C_O = 44 \mu\text{F}$ ($22 \mu\text{F} \times 2$)

Phase Margin	Ringling Cycle
10 deg	≥ 10
19 deg	4
38 deg	3
60 deg	3
85 deg	3

Table 1 Results of Tests to Establish Relationship between Phase Margin and Ringling Cycle

Conclusion

The relationship between the phase margin and ringing cycle is tabulated in Table 1 for the waveforms obtained from the tests. These tests suggested that phase margin, in terms of the relative stability of a closed loop, should be maintained at points where the ringing cycle stays stable below three.

When estimating circuit stability based on the relationship between phase margin and ringing cycle, it must be noted that measurements may vary depending on the impedance of the power source in the stage preceding the circuit, the status of the load current, and the properties of the components in use.

The measurements of phase margin and ringing cycle shown in Table 1 are specific to the circuit used for the tests, therefore it would be inappropriate to apply the values to other circuits. Some circuits behave stably even when a lot of ringing artifacts exist. The results of the tests suggest a probable relationship between the ringing and phase margin, i.e., the less the phase margin is, the more the ringing artifacts exist, and should be considered as one of the means for estimating circuit stability.

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